THIN-FILM SEMICONDUCTOR DEVICE AND LIQUID CRYSTAL DISPLAY

BACKGROUND OF THE INVENTION

1. Field of the Invention

[01] The present invention relates to a thin-film semiconductor device and a liquid crystal display (LCD), and more particularly, to a thin-film semiconductor device and LCD provided with a plurality of thin-film transistors (TFTs) having different driving voltages.

2. Description of the Related Art

[02] An image display such as an LCD or an organic EL display is used as a monitor of a notebook-type personal computer or a portable terminal device such as a cellular phone or a mobile device. For example, in an active matrix-type LCD, TFT is formed of poly-crystalline silicon by arraying a matrix of picture elements on a glass substrate and the TFT is driven by a driver circuit such as an external gate driver or a data driver. Therefore, an active matrix-type LCD displays an image thereon by controlling a orientation of the liquid crystal.

[03] Recently, along with downsizing of the portable terminal device, in an image display a method has been developed for forming a driver circuit, an amplifier circuit, etc. integrally on a glass substrate without mounting them externally thereto. In the case of the LCD in which the driver circuit is mounted integrally, these circuits are formed simultaneously with the TFTs that are formed in the picture elements as switching elements.

[04] These switching TFTs and driver circuit are constituted of two types of TFTs, N-channel and P-channel ones. The TFTs are driven under various conditions, including high and low driving voltages. In the case of the driver circuit, for example, the driving voltage for a scanning line is different from that for a data line, and the breakdown voltage required for the

respective TFTs is different depending upon the driving voltage. To improve performance of a relevant LCD, it is necessary to form TFTs to be suited for the various driving voltages at a high throughput.

[05] For this purpose, there has been a method available to alter a thickness of a gate insulating film in order to adjust the breakdown voltage of the transistors. Fig.1 shows a cross-sectional view of two types of transistors having different film thicknesses of the gate insulating films on a silicon substrate. As shown in Fig.1, a thickness of a gate insulating film 201 between a gate electrode 203 and a channel-active layer 205 of the transistor is different from that of a gate insulating film 202 between a gate electrode 204 and a channel-active layer 206 of the other transistor. A thickness of the gate insulating film of the right-side transistor in Fig.1 is formed larger than that of the left-side transistor, in order to accommodate a higher drain voltage taking into account gate and drain breakdown voltages of the transistor.

[06] However, in order to form the TFTs as shown in Fig.1, it is necessary to form each gate insulating film separately for transistors including p-type and n-type having different breakdown voltage, thereby resulting in a complicated process. Moreover, the transistor having a higher drain voltage, as shown on the right side of Fig.1, needs to have a Lightly Doped Drain (LDD) structure containing a lightly-doped drain region, thereby further complicating the process.

SUMMARY OF THE INVENTION

[07] An object of the present invention is to provide a thin-film semiconductor device and an LCD provided with high-voltage/low-voltage TFTs at a high throughput without complicating the process.

[08] According to a first aspect of the present invention, a thin-film semiconductor device comprises a plurality of thin-film transistors (TFTs) having different driving voltages formed on an glass substrate, wherein a gate electrode electric field at each of the driving voltages of the plurality of thin-film transistors is in a range of about 1MV/cm to 2MV/cm, and a drain concentration of p-type thin-film transistors (TFT) is in a range of about $3E+19/cm^3$ to $1E+20/cm^3$. Here the drain concentration means atomic density as well as the carrier concentration for electric conductivity. Ordinarily impurities are doped in a range of atomic density and activated appropriately, such that the atomic density is substantially similar to the carrier concentration. However, even if the atomic density and the carrier concentration are not substantially similar, the range of the atomic density of about $3E+19/cm^3$ to $1E+20/cm^3$ can assist the effect of the present invention.

[09] Thus, according to the present invention, it is possible to form simply a plurality of thin-film transistors (TFTs) having different driving voltages formed on an glass substrate by setting the range of the gate electrode electric field and drain concentration. The range of the gate electrode electric field may be in the range of 1MV/cm to 2MV/cm, and the range of the drain concentration of the P-type TFTs may be in the range of $3E+19/cm^3$ to $1E+20/cm^3$. In other words, it is possible to provide a plurality of TFTs in a greatly improved throughput, by regulating a gate electrode electric field and a drain concentration of P-type TFTs rather than by changing the gate insulating film for each type of TFTs.

[10] According to a second aspect of the present invention, a thin-film semiconductor device comprising a thin-film semiconductor device comprising a plurality of thin-film transistors (TFTs) having a lower driving voltage and thin-film transistors having a higher driving voltage on an glass substrate, wherein all gate insulating films of the thin-film

transistors are substantially the same film thickness and wherein a drain concentration of thin-film transistors (TFT) is in a range of about $3E+19/cm^3$ to $1E+20/cm^3$.

[11] Thus, according to the present invention, it is possible to form a plurality of thin-film transistors (TFTs) having a lower driving voltage and thin-film transistors having a higher driving voltage on a glass substrate at a single gate insulating film by setting the range of drain concentration. The range of the drain concentration of the P-type TFTs may be in the range of $3E+19/cm^3$ to $1E+20/cm^3$. Therefore, it is possible to simplify the process of forming at least two types of TFTs having different driving voltages on an insulting glass substrate, thereby resulting in a greatly improved throughput.

[12] According to a third aspect of the present invention, a thin-film semiconductor device manufacturing method comprises forming substantially the same thickness of gate insulating films of a plurality of thin-film transistors (TFTs) having different driving voltages formed on a glass substrate at one time. Thus, according to the present invention, it is possible to form a plurality of thin-film transistors (TFTs) having different driving voltage on an glass substrate at a single gate insulating film. Therefore, it results in a greatly improved throughput.

BRIEF DESCRIPTION OF THE DRAWINGS

[13] Fig. 1 is the cross-sectional view showing a conventional structure of a semiconductor.

[14] Fig. 2 is a cross-sectional view showing a structure of a thin-film semiconductor device related to a first embodiment of the present invention.

[15] Figs. 3 (a) and (b) are cross-sectional views showing steps of a manufacturing method of the present invention.

[16] Figs. 4 (a) through (c) are cross-sectional views showing steps of a manufacturing method of the present invention.

[17] Figs. 5 (a) and (b) are cross-sectional views showing steps of a manufacturing method of the present invention.

[18] Figs. 6 (a) through (c) are cross-sectional views showing steps of a manufacturing method of the present invention.

[19] Fig. 7 is a cross-sectional view showing a structure of a thin-film semiconductor device related to a second embodiment of the present invention.

DETAILED DESCRIPTION OF THE INVENTION

[20] [First embodiment]

[21] Fig. 2 shows a cross-sectional view showing a structure of a thin-film semiconductor device comprising a plurality of TFTs having different driving voltages related to a first illustrative embodiment of the present invention. Fig. 3 through Fig. 6 show cross-sectional view showing steps of a manufacturing method of the thin-film semiconductor device of the first embodiment in the present invention.

[22] As shown in Fig. 2, an undercoat layer 102 is formed on a glass substrate 100, and amorphous or poly-crystalline silicon films 106-109 are formed on the undercoat layer. The gate insulating films 114-117 are provided on the amorphous or poly-crystal silicon films 106-109, and gate electrodes 110-113 are formed over the respective channel regions.

[23] The glass substrate 100 may be on a transparent insulating substrate made of glass or plastic, a silicon oxide film (SiOx). The undercoat layer 102 is provided to prevent an impurity from being diffused from the glass substrate 100 into an active layer and so it is not necessary

to form the undercoat layer if an influence of the impurity is negligible. The thickness of the insulating layer is set in that an electric field of a gate electrode at each of the driving voltages may be in a range of about 1MV/cm to 2MV/cm or any part thereof on the each silicon film 106-109 may be substantially same.

[24] The regions 106a, 106b, 107a and 107b of the silicon films 106-109 are doped with a P-type dopant, while the regions 108a, 108b, 109a, 109b, and 101 thereof are doped with an N-type dopant. The drain concentration of p-type TFTs 106b and 107b are set in the range of $3E+19/cm^3$ to $1E+20/cm^3$ because if the drain concentration is larger than $1E+20/cm^3$, a leakage current cannot be ignored. On the other hand, if it is not larger than $3E+19/cm^3$, poor Ohmic contact occurs to give rise to parasitic resistance of the transistor and hence a bad characteristic. Thus, by setting the range of the drain concentration of p-type TFTs properly, TFTs of four different types (low-voltage P-type, high-voltage P-type, low-voltage N-type, and high-voltage N-type TFTs) can be formed on a glass substrate with a gate insulating film thickness.

[25] The reference numeral 101 indicates a lightly-doped region that serves to reserve a drain breakdown voltage of the high-voltage N-type TFTs. This structure is referred as lightly doped drain (LDD) structure. The N-type TFTs employ the LDD structure for their operation at a high voltages to thus reserve a sufficient breakdown voltage even at a high voltages, so that resultantly they can use a gate insulating film set in the range of 1MV/cm to 2MV/cm or having the same film thickness as that for the P-type TFTs.

[26] The thin-film semiconductor device having such a configuration can be manufactured by the following method. First, on a glass substrate 100 a silicon nitride film (SiNx), for

example, is formed by Low-Pressure Chemical Vapor Deposition (LPCVD), Plasma-Enhanced CVD (PCVD), sputtering, etc. as an undercoat layer 102.

[27] Next, amorphous silicon (hereinafter abbreviated as a-Si) film is formed by LPCVD, PCVD, sputtering, etc. as an active layer. On the a-Si film, a resist pattern is formed by a photolithographic process to perform channel doping by ion injection or ion doping. The a-Si film is annealed using an excimer laser beam (ELA) and crystallized in order to form a poly-crystal silicon film. Then, the island-patterned silicon films 106-109 are formed by photolithographic process (Fig.3(a)).

[28] Next, silicon oxide films are formed as the gate insulating films 114-117 by LPCVD, PCVD, sputtering, etc. In the conventional method, the gate insulating films must be partially formed and etched in a process because the film thicknesses of the gate insulating films need to be altered in accordance with the driving voltages of the TFTs. On the other hand, by the method of the present invention the gate insulating films 114-117 can be formed in the same process because it is possible to regulate the electric field of the gate electrode and the drain concentration of the P-type TFTs (Fig.3(b)).

[29] Then, a material containing an N-type impurity is deposited by PCVD, sputtering, etc. and patterned by a photolithographic process to form the gate electrodes 110-113 (Fig.4(a)). The gate electrode material may be poly-silicon, aluminum, chromium, tungsten silicide, chromium, molybdenum, copper, titanium, tantalum, etc.

[30] Next, regions in which the P-type TFTs are to be formed are covered by a resist pattern and phosphorus (P) is doped into the N-type TFTs using the gate electrodes 112 and 113 as a mask (Fig. 4(b)). The regions 108a, 108b, 109a, and 109b are formed. Subsequently, regions in which the N-type TFTs are to be formed are covered by a resist pattern and boron (B) is

doped similarly into the P-type TFTs using the gate electrodes 110 and 111 as a mask (Fig. 5(a)). Thereby source/drain regions 106a, 106b, 107a, and 107b are formed (Fig. 5(b)). In this case, the drain concentration of the P-type TFTs is set in a range of $3E+19/cm^3$ to $1E+20/cm^3$ as described above. It is to be noted that doping may be performed on the N-type TFTs and the P-type TFTs in this order or a reversed order arbitrarily.

[31] Then, in the case of forming the LDD structure to increase the reliability of the device in a high electric field region in the neighborhood of the drain, as shown in Fig. 6(a) through (c), P is injected at a low concentration using the gate electrode 113 as the mask after the impurity is injected with the gate as offset using the resist pattern 118. Then, the lightly-doped region 101 is formed by thermal activation, laser activation by use of a laser beam, Rapid Thermal Annealing (RTA) by use of a lamp or hot N_2, etc.

[32] Subsequently, after hydrogen plasma processing is performed, a silicon oxide film, silicon nitride film, etc. are deposited as an inter-layer insulation film. Next, a contact hole is formed in the gates and the sources/drains and metal is deposited to form the electrodes and wire. Then, a silicon nitride film, for example, is formed as a passivation film and a pad contact hole is formed therein. Thus the TFT device is manufactured.

[33] In contrast to the conventional structure, in the present embodiment, it is possible to form TFTs having a different breakdown voltage by regulating a film thickness and a drain concentration of the P-type TFTs.

[34] Furthermore, in the conventional structure it is necessary to form the gate insulating films of the high-voltage and low-voltage TFTs in different film thicknesses and, therefore, to perform gate insulating film formation twice and etching once. However, in the present invention these complicated steps can be avoided, enabling to be formed the TFTs having

different driving voltages by using the same gate insulating film, thereby resulting in simplification of the manufacturing process.

[35] Furthermore, by employing the LDD structure at least on the high-voltage N-type TFTs, it is possible to form the N-type TFTs by using the same gate insulating film as that of the P-type TFTs, thereby simplifying the manufacturing process and improving throughput.

[36] By manufacturing an image display such as an LCD or an organic EL display by using the substrate on which TFTs having different breakdown voltages are formed, it is possible to set operations of circuits optimally, thereby improving performance of the image display.

[37] The gate electrodes 110, 111, 112, and 113 of Fig. 2 can be formed of a material containing an N-type impurity or a P-type impurity.

[38] Further, while the present invention describes a low-concentration impurity region 101 provided in the drains of the high-voltage N-type TFTs, the low-concentration impurity region 101 may also be provided also in the source regions. Even in such a case, no additional step is required, thereby avoiding preventing an improvement in throughput.

[39] [Second embodiment]

[40] Fig.7 shows a cross-sectional view of a thin-film semiconductor device related to a second illustrative embodiment of the present invention.

[41] The second embodiment is different from the first embodiment in that the electric field of the gate electrode is regulated to a range of 0.2MV/cm to 0.8MV/cm. By reducing the upper limit to 1MV/cm or less, it is possible to manufacture the high-voltage and the low-voltage N-type and P-type transistors by self-alignment with a gate insulating film without providing the region 101 additionally. Such a structure makes it possible to further eliminate a step required to provide the light-doped region 101, thereby simplifying the manufacturing process further.